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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/617,454	07/10/2003	Anssi Haverinen	878.0034.U1(US)	3229

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EXAMINER	
PATEL, NIKETA I	
ART UNIT	PAPER NUMBER
2181	

DATE MAILED: 02/28/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/617,454	HAVERINEN ET AL.	
	Examiner	Art Unit	
	Niketa I. Patel	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 November 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4 and 6-14* is/are rejected.

7)☒ Claim(s) *5* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/26/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-4 and 6-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Horng et al. U.S. Patent Number: 6,738,788 B1 (hereinafter "*Horng*") and further in view of Dabral et al. U.S. Patent Number: 6,192,431 B1 (hereinafter "*Dabral*".)

3. **Referring to claims 1, 13-14,** *Horng* teaches a method and a data handling device [see column, lines and figure 1, element 14] capable of operating in a system in which two or more devices [see column 1, lines 18-22, 'ICs' and figure 1, element 10] are connected by a data bus for the transmission of communications there between, an identity acquisition unit [see column 4, lines 52-62 and figure 1, element 12] capable of functioning in a first mode of operation of the device to receive data transmitted over the data bus and in response to the order in which the bits of one or more data words of a predetermined form are received on the data bus connectors during the first mode of operation determine an identity for the device and store the identity in an identity store of the device [see column 4, lines 34-62], and a data handling unit capable of functioning in a second mode of operation of the device to handle communications transmitted over the bus and that specify the identity stored in the data store as a destination [see column 4, lines 63-65 and column 5, lines 27-36 and figure 1, elements 14, 20.] *Horng* is silent regarding the data bus having two or more data lines and the device having: two or more data bus

connectors, each for connection to a respective data line of the data bus [see column, lines] however, *Dabral* teaches these limitations [see *Dabral* column 1, lines 33-37.]

One or ordinary skill in the art at the time of applicant's invention would have clearly recognized that it is quite advantageous for the integrated circuit of *Horng* to have two or more data lines connected to respective connectors in order to allow the IC to communicate with other elements. It is for this reason that one of ordinary skill in the art would have been motivated to use IC with two or more data lines connected to respective connectors in order to allow the IC to communicate with other elements.

4. **Referring to claim 2**, teachings of *Horng* as modified by the teachings *Dabral* teaches wherein the identity acquisition unit is arranged to process the or each data word of a predetermined form in accordance with a look-up table in order to determine the identity for the device [see *Horng* column 4, lines 34-62, 'database' and column 3, lines 42-49, 'database system'.]

5. **Referring to claim 3**, teachings of *Horng* as modified by the teachings *Dabral* teaches comprising a multiplexing arrangement located between the data bus connectors and the data handling unit and arranged to, in at least the second mode of operation, re-order in accordance with the stored identity data received from at least two of the data lines of the bus and passed to the data handling unit [see *Dabral* figure 1a, elements 112, 'multiplexers,' 121, 111, 120, 110.]

6. **Referring to claim 4**, teachings of *Horng* as modified by the teachings *Dabral* teaches wherein the multiplexing arrangement is a hardware multiplexing arrangement [see *Dabral* figure 1a, element 112, 'multiplexers'.]

7. **Referring to claim 7**, teachings of *Horng* as modified by the teachings *Dabral* teaches wherein the device is a memory device [see *Horng* column 1, lines 18-22, 'ICs' and figure 1, element 10.]

8. **Referring to claim 8**, teachings of *Horng* as modified by the teachings *Dabral* teaches wherein the device is defined on an integrated circuit and the data bus connectors are connectors for communicating to and/or from the integrated circuit [see *Horng* column 1, lines 18-22, 'ICs' and figure 1, element 10 and *Dabral* figure 1a, elements 112, 'multiplexers,' 121, 111, 120, 110.]

9. **Referring to claim 9**, teachings of *Horng* as modified by the teachings *Dabral* teaches the data handling system comprising two or more data handling devices, interconnected by the said data bus [see *Horng* column 1, lines 18-22, 'ICs' and figure 1, element 10.]

10. **Referring to claim 10**, teachings of *Horng* as modified by the teachings *Dabral* teaches comprising a further device connected to the bus and capable of functioning to transmit the said one or more data words of a predetermined form over the data bus [see *Dabral* column 1, lines 33-43 and figure 1a, elements 112, 'multiplexers,' 121, 111, 120, 110.]

11. **Referring to claim 11**, teachings of *Horng* as modified by the teachings *Dabral* teaches wherein the further device is capable of triggering the data handling devices to enter the first mode of operation [see column 4, lines 34-62 and column 1, lines 14-37.]

12. **Referring to claim 12**, teachings of *Horng* as modified by the teachings *Dabral* teaches wherein the data handling devices are arranged to automatically enter the first mode of operation an initialization of the system [see column 4, lines 34-62 and column 1, lines 14-37.]

Response to Arguments

13. Applicant's arguments, see pages 8-9, filed 11/30/2005 (regarding claims 1-2, 9, 13) have been fully considered but they are not persuasive. The applicant argues that the *Horng* reference does not teach (1) chip identification number are not generated in response to the order in which the bits of one or more data words of a predetermined form are received on the data bus connectors during the first mode of operation determining an identify for the device and (2) wherein the identity acquisition unit is arranged to process the or each data word of a predetermined form in accordance with a look-up table in order to determine the identity for the device. The examiner respectfully disagrees with these arguments.

As per the first argument, *Horng* teaches that the chip identification number are generated in response to the order in which the bits of one or more data words of a predetermined form are received on the data bus connectors during the first mode of operation determining an identify for the device and [see column 4, lines 34-62.]

Furthermore, the examiner would like to point out that determining address/ID based on the order of the bits in one or more data word is well know in the computer art, please see pages 622-624 of the "Logic and Computer Design Fundamentals" by M. Morris Mano and Charles R. Kime. Figure 14-3 shows that the order of bits in a word determines the address.

As per the second argument, *Horng* teaches wherein the identity acquisition unit is arranged to process the or each data word of a predetermined form in accordance with a look-up table in order to determine the identity for the device [see *Horng* column 4, lines 34-62, 'database' and column 3, lines 42-49, 'database system'.]

14. Applicant's argument, see page 9, filed 11/30/2005, with respect to claim 5 have been fully considered and are persuasive. The rejection of claim 5 has been withdrawn.

Allowable Subject Matter

15. Claim 5 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: the prior art of record taken alone and/or in combination with other does not teach and/or fairly suggest the limitation of wherein the identity acquisition unit is arranged to determine the identity in accordance with a deviation in the order of at least some of the bits of each of the one or more data words from a standard order, and the multiplexing arrangement is arranged to re-order the data lines of the bus so as to restore the standard order to the bits as applied to the data handling unit, in combination with other limitation that are cited in the base claim and in the intervening claim.

Conclusion

16. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Niketa I. Patel whose telephone number is (571) 272 4156. The examiner can normally be reached on M-F 8:00 A.M. to 5:00 P.M.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim Huynh can be reached on (571) 272 4147. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

NP
02/18/2006

KIM HUYNH
SUPERVISORY PATENT EXAMINER
2/21/06